1.2 System Board Layout

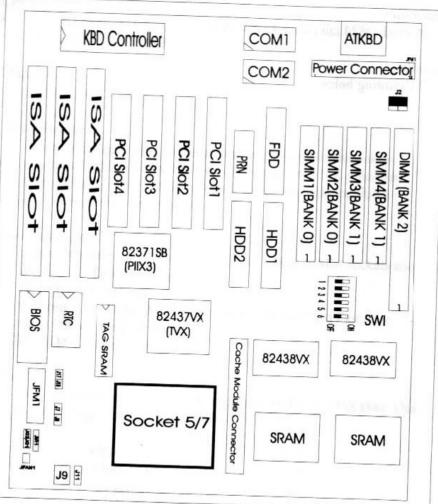


Figure 1-1

Chapter 2 HARDWARE INSTALLATION

2.1 CPU INSTALLATION

After install CPU, adjust SW1 to set CPU SPEED, J7, J8, J9, J11, J17 and J18 to set CPU voltage, and insert CPU fan power cable to JFAN1 to complete CPU installation. (See section 2.1.1, 2.1.2, and 2.1.3)

2.1.1 CPU SPEED SETTING (SW1)

Adjust SW1 (Dip switch) to set CPU speed. Figure 2-1 show SW1 location.

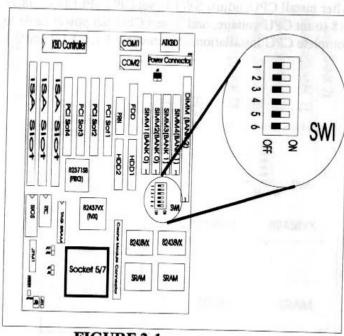


FIGURE 2-1

2.1.1.1 INTEL P54C ~ P55C CPU SPEED SETTING

CPU Type	CPU Speed SWI
P54C-75	ON DIF ON OFF
P54C-90	ON OFF
P54C-100	ON ON OFF
P54C-120	ON OFF
P54C-133	ON OFF
P54C-150	ON DIF ON OFF
P54C-166	ON OFF
P55C-166	ON OFF
P54C-200	ON DIF ON OFF
P55C-200	ON DIF ON OFF
P55C-233	ON OFF

2.1.1.2 CYRIX 6x86 ~ 6x86L CPU SPEED SETTING

CPU. Type	CPU Speed
P120+(100MHz)	SW1
P133+(110MHz)	ON DIF ON OFF
P150+(120MHz)	ON ON CFF
P166+(133MHz)	ON OFF

2.1.1.3 AMD 5k86 ~ K6 CPU SPEED SETTING

CPU	CPU Speed	
Type	SW1	
P75(75MHz)	ON DIF ON OFF	
P90(90MHz)	ON ON OFF	
P100(100MHz)	ON DIP ON OFF	
P133(133MHz)	ON ON ON OFF	
P166(166MHz)	ON DIP ON OFF	
P200(200MHz)	ON DIP ON OFF	

Note 1: The 4 Host Clock frequencies that the system supports are 50MHz, 55MHz, 60MHz, and 66.6MHz.(by adjusting SW1 pin 1,2,3,and 4). See the following chart to set the different Host Clock frequencies.

HOST CLK	SW1 Settings	
50MHZ	1 2 3 4	ON OFF
55MHZ	1 2 3 4	ON OFF
60 MHZ	1 2 3 4	ON OFF
66MHZ	1 2 3 4 5 6	ON OFF

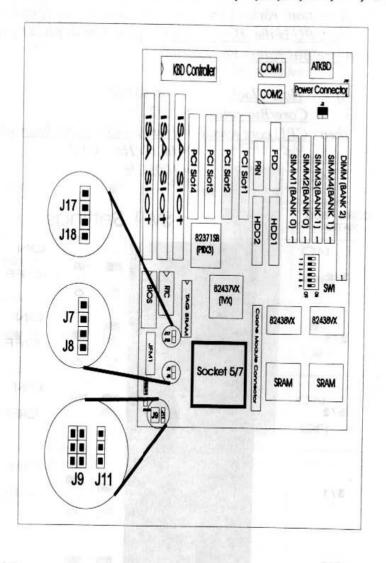
Note 2: The DIP Switch SW1 (5,6) is used to set the Core/Bus (Fraction) ratio of the CPU. The actual core speed of the CPU is the Host Clock Frequency multiplied by the Core/Bus ratio. For example:

if $\frac{Host\ Clock}{Core/Bus\ ratio} = 66.6MHz$ $\frac{Core/Bus\ ratio}{CPU\ core\ speed} = \frac{Host\ Clock}{ERS\ ratio} \times \frac{Core/Bus\ ratio}{ERS\ ratio} = 66.6MHz \times 3/2$ = 100MHz

CORE / BUS RATIO	SW1 Settings	
3/2	ON OFF 5 6	
2/1	ON OFF	
5/2	ON OFF	
3/1	ON OFF 5 6	
7/2	ON OFF	

Note 3: The PCI Bus Clock is the Host Clock Frequency divided by 2.

2.1.2 CPU VOLTAGE SETTING (J7,J8,J9,J11,J17,J18)



2.1.2.1 For P54C, J7, J8, J9, J11, J17, J18 setting is as below.

CPU VOLTAGE	J7,J8 JUMPER SETTING	
3.38V	J7 = J8 =	
3.52V	J7 📕	

J17 =
J18 =

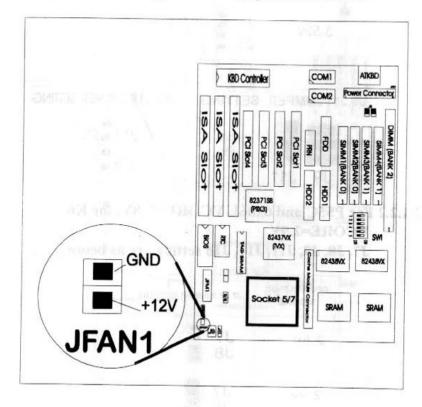
2.1.2.2 For P55C and 6x86L VCORE=2..8V, for K6 VCORE=2.9V J7, J8, J9, J11, J17, J18 setting are as below:

VCORE	J7,J8 JUMPER SETTING	
2.8V	J7 = 18	
2.9V	J7 💂 J8 💂	

J9,J11 JUMPER SETTING	J17,J18 JUMPER SETTING
J9 J11	J17 = J18 =

2.1.3 CPU FAN POWER CONNECTOR (JFAN1)

JFAN1 connector support +12V voltage for CPU fan use.

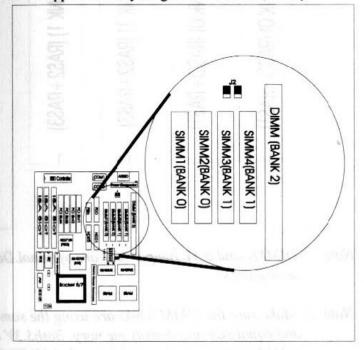


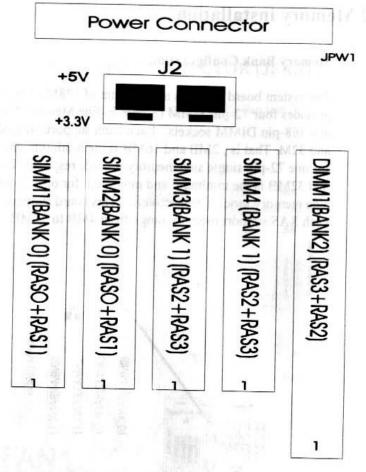
JFAN1 GND +12V

2.2 Memory installation

Memory Bank Configuration

The system board supports a maximum of 128M of memory, and provides four 72-pin SIMM (Single In-line Memory Module) and one 168-pin DIMM sockets. Each bank supports 4M, 8M, 16M, and 32M. That is, 2MB and 16MB is the minimum and maximum for one 72-pin single side memory module respectively, and 4MB and 32MB is the minimum and maximum for one 72-pin double side memory module respectively. (This board support 4 RAS, each RAS support memory range from 4MB to 32MB.)



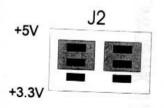


Note: 1 DIMM1 and 3.3V jumper (J2) are optional. Default setting is 5V.

Note 2: Make sure the SIMM banks are using the same type and equal size and density memory. Both3.3V and 5V SIMM memory can be used ,but only3.3V SIMM memory should be used if DIMM memory is installed in the system.

Note3:To operate properly at least two 72-pin SIMM module must be installed in the same bank or the one 168-pin

Note 5: The DIMM bank supports 3.3V EDO, 3.3V FP, and, unbuffered 3.3V SDRAM. Be sure to adust the J2, jumpers to the 3.3V position before installing DIMM memory. Below, describe J2 jumper settings on 3.3V and 5V position respectively.



+5V SETTING

J2 +5V +3.3V

+3.3V SETTING

Note 6: This mainboard supports Table Free so memory can be installed on Bank 0 (SIMM1 + SIMM2), Bank 1 (SIMM3 + SIMM4), or Bank 2 (DIMM1).

Note7: If the SIMM memory is 3.3V the following combinations are O.K. (Remember to adjust J2 to 3.3V settings.)

S=Single D=Double X=Not Installed

SIMM1+SIMM2 Bank 0	SIMM3+SIMM4 Bank 1	DIMM1 Bank 2
S	X	X
S	S	X
S	S	S
S	X	S
S	D	X
S	X	D
D	X	X
D	S	X
D	S	S
D	bno Nativ Mar	X XXS
D	D	X
D	X	bound on a
X	S	Abore X
X	S	S
X	X	S
X	D	X
X	X	D

2.3 Cache memory configuration

Cache Selection

The system board supports 256K of cache memory on board. Suitable on board TAG SRAM are as follows:

8K X 8 SRAM Winbond W2465AK-15 16K X 8 SRAM Winbond W24128AK-15 16K X 8 SRAM Winbond W24129AK-15 32K X 8 SRAM Winbond W24257AK-15

The system board can support 512K of Cache memory (256K on board + 256K Cache Module). On board suitable Tag SRAM are as follows:

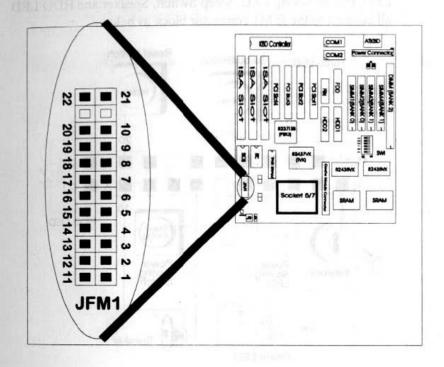
8K X 8 SRAM Windbond W2465AK-15

Note: Cache module connector is optional.

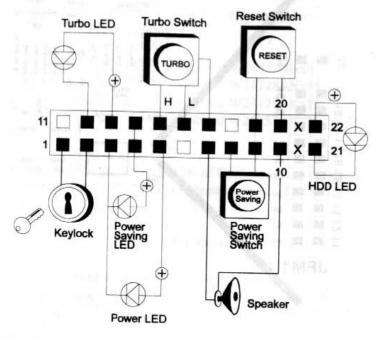
Note: Cache module must meet COAST spec. 1.3 or later to

upgrade to 512k.

2.4 Case connector (JFM1)



The Turbo LED, Turbo Switch, Hardware Reset, Key lock, Power LED, Power Saving LED, Sleep Switch, Speaker, and HDD LED all connect to the JFM1 connector block as below.



Note: The hardware Turbo switch is not functional. The Turbo LED is always ON and cannot be toggled.

2.5 Power Saving Switch Connector:

Attach a power saving switch to this connector. When the switch is pressed, the system goes immediately into suspend mode. Press any key and the system wakes up.

Note: you should enable the Power Management Mode (At Bios Setup) to use this function.

